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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,788	01/15/2004	Thomas Michael Gooding	ROC920030335US1	5462

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IBM CORPORATION
ROCHESTER IP LAW DEPT. 917
3605 HIGHWAY 52 NORTH
ROCHESTER, MN 55901-7829

EXAMINER	
THORNEWELL, KIMBERLY A	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 05/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/757,788	GOODING ET AL.	
	Examiner	Art Unit	
	Kimberly Thornewell	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-16 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-16 are pending in the instant application.

Claim Objections

2. Claim 3 is objected to because it is dependent from itself. The claim has been interpreted to be dependent from claim 1.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claims 13-16 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claim 13 is directed to software, per se. Furthermore, the claimed computer-readable medium on which the program is stored is described in the disclosure as signal-bearing media. Therefore the tangible embodiment of the invention could be interpreted as being carried out on an intangible medium.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Swoboda, US Patent no. 6,928,403, in view of Knox et al., US Patent no. 5,448,572.

As per claim 1, Swoboda discloses a logic simulation hardware emulator, comprising:

i. *a simulation model comprising one or more source emulation processors* (column 9 lines 11-16, source processors being located on the emulation controller) *coupled to one or more receiving emulation processors* (column 9 lines 38-41, receiving processors being located on the target devices) *by an emulation cable having a plurality of signal wires* (column 9 lines 30-31)*, the plurality of signal wires comprising a plurality of regular signal wires* (column 9 lines 31-33, defined as the pins that carry Debug, Trace, Triggers, and RTDX) *and one or more spare signal wires* (column 10 lines 45-47, taught as not necessarily all pins being used)*; and*

ii. *a runtime control program for controlling the simulation model* (column 8 lines 43-44).

Swoboda does not disclose expressly the runtime control program detecting faults on wires. Knox discloses a method for *detecting a fault on a regular signal line, and reassigning the signal on the faulty line to a spare signal wire* (column 3 lines 4-10).

It would have been obvious to one of ordinary skill in the art of redundant circuit design, at the time of the present invention, to modify Swoboda's emulation system already containing spare pins with Knox's method of rerouting data through spare wires in the event of a fault to achieve the claimed invention. The motivation for doing so would have been to reduce propogation time by allowing Swoboda to automatically recover from failure by blocking faulty lines and rerouting data through pre-allocated spare wires (column 2 lines 9-12).

As per claim 2, Swoboda discloses the defining *of all wires at simulation model build time* (column 8 lines 44-53).

As per claim 3, Knox teaches *designating one of the processors and its corresponding wire as faulty during build time* as changing the Fault Register, which designates the wires as regular or faulty, only when the system is reconfigured (column 3 lines 39-43).

As per claim 4, Knox teaches the use of a *spare select multiplexer* (figure 2A reference 206), *the inputs of which are coupled to the outputs of the source* (column 2 lines 49-52), *the outputs of which are coupled to the input of the cable* (figure 2a reference lines 1-5), *which multiplexes the signal on the faulty wire through the spare signal wire* (figure 2a reference line 6).

As per claim 5, Knox discloses the *signal select for the spare select multiplexer being provided by a spare select register* (taught as the Fault Register, column 3 lines 18-24).

As per claim 6, Knox discloses the spare select register (Fault Register) being *updated by the runtime control program during the simulation run* (taught as being loaded by the error correction logic, column 3 lines 27-31).

As per claim 7, Swoboda teaches the emulation system further comprising:

a plurality of processor selector multiplexers (figure 5 references 62 and 63), *wherein the output of each processor selector multiplexer is coupled to an input to the receiving emulation processors* (figure 5 reference 65), *and wherein each of the processor selector multiplexers has a select signal* (figure 5 reference 4).

Swoboda does not disclose expressly the use of source type multiplexers. Knox discloses *source type multiplexers coupled to an output of the emulation cable* (figure 2a references 230, 232, 234, 236, 238), *wherein each of the source type multiplexers has a select signal (*figure 2a references sel1, sel2, sel3, sel4, sel5).

As per claim 8, Swoboda discloses the select signals for the *processor selector multiplexer being provided by the runtime control program* (column 10 lines 23-33). Knox discloses the select signals for the *source type multiplexer being provided by the runtime control program* (column 3 lines 10-13).

As per claims 9 and 13, Swoboda discloses a method and computer program for the reconfiguration of faulty signal wires in a logic simulation hardware emulator, the logic simulation hardware emulator having one or more source emulation processors (column 9 lines 11-16, source processors being located on the emulation controller) coupled to one or more receiving emulation processors (column 9 lines 38-41, receiving processors being located on the target devices) by a set of emulation cables, each emulation cable having a plurality of signal wires (column 9 lines 30-31), the plurality of signal wires comprising a plurality of regular signal wires (column 9 lines 31-33, defined as the pins that carry Debug, Trace, Triggers, and RTDX) and one or more predefined spare signal wires (column 10 lines 45-47, taught as not necessarily all pins being used).

Swoboda does not disclose expressly the steps of identifying faulty signal wires, or reassigning signals in the event of a fault. Knox discloses

i. *identifying a set of faulty signal wires within the plurality of regular signal wires, if any faulty signal wires exist* (column 3 lines 4-7)*; and*
ii. *reassigning signals from the set of faulty signal wires to the spare signal wire within the emulation cables* (column 3 lines 7-10).

It would have been obvious to one of ordinary skill in the art of redundant circuit design, at the time of the present invention, to modify Swoboda's emulation system already containing spare pins with Knox's method of rerouting data through spare wires in the event of a fault to achieve the claimed invention. The motivation for doing so would have been to reduce propogation time by

allowing Swoboda to automatically recover from failure by blocking faulty lines and rerouting data through pre-allocated spare wires (column 2 lines 9-12).

As per claims 10 and 14, Swoboda discloses *performing a connectivity diagnostic on the set of emulation cables within the hardware emulator* (column 9 lines 55-59).

As per claims 11 and 15, Swoboda discloses the predefining *of all wires at simulation model build time* (column 8 lines 44-53).

As per claims 12 and 16, Knox discloses the step of reassigning signals from the faulty wires to the spare signal wire including the steps of:

i. *determining if a spare signal wire is available, if one or more faulty signal wires exist* (column 3 lines 10-18);

ii. *setting a source module spare register to a value corresponding to the source emulation processor having the faulty wire* (column 3 lines 22-26); *and*

iii. *changing any receiving emulation processor steps sourced by the faulty wire to the spare wire* (column 3 lines 27-37).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

i. US Pregrant Pub no. 2001/0020224, filed by Tomita on 1/19/2001, is directed to a circuit emulation system which uses multiplexers to select the inputs to the target devices.

ii. US Patent no. 5,361,249, issued to Monastra et al. on 11/1/1994, is directed to a fault tolerent communication system which reroutes data in the event of a fault.

iii. US Patent no. 5,729,527, issued to Gerstel et al on 3/17/1998, is directed to a method for rerouting failed channels in a communication system.

iv. US Pregrant Pub no. 2003/0095502, filed by Glaser et al on 11/21/2001, is directed to the use of muxes and redundant circuits to choose a transmisson path.

v. US Patent no. 6,944,425, issued to Fallenstein on 9/13/2005, is directed to use of redundant circuittry in the use of wireless diagnostics.

vi. US Patent no. 5,958,063, issued to Croslin et al on 9/28/1999, is directed to the use of redundant circuitry to reroute data being transmitted through faulty wires.

vii. US Patent no. 4,722,084, issued to Morton on 1/26/1988, is directed to array reconfiguration within VLSI circuits.

viii. US Patent no. 5,229,990, issued to Teraslinna on 7/20/1993, is directed to the use of spare lines in the event of a fault in a telecommunications environment.

ix. US Patent no. 5,963,736, issued to Sarno et al on 10/5/1999, is directed to reconfigurable emulation pods.

x. US Patent no. 5,734,581, issued to Butts et al on 5/31/1998, is directed to reconfigurable interconnects in a simulation system.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kimberly Thornewell whose telephone number is (571)272-6543. The examiner can normally be reached on 8am-4:30pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571)272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kimberly A. Thornewell
Patent Examiner
Art Unit 2128

KAMINI SHAH
SUPERVISORY PATENT EXAMINER